What is claimed is:

1. A method of managing utilization of an integrated circuit (IC) processor, comprising:

monitoring processor utilization by an adjustable software program having at least two different performance levels associated with data processing quality of said adjustable software program, wherein each performance level has a different associated IC processor utilization; and

selecting a performance level of said adjustable software program to maintain IC processor utilization for said adjustable software program within control constraints on IC processor utilization.

2. The method of claim 1, wherein said selecting said performance level comprises:

selecting a highest performance level for highest quality compatible with a constraint of maintaining a minimum idle thread utilization over a range of operating conditions.

3. The method of claim 2, further comprising: selecting said minimum idle thread utilization to facilitate another software program to start.

4. The method of claim 2, further comprising: selecting said minimum idle thread utilization to facilitate another software program to execute.

5. The method of claim 1, wherein said selecting a performance level comprises:

selecting a highest performance level compatible with the constraint of maintaining IC processor utilization of said adjustable software program within a range having a minimum utilization and a maximum utilization.

6. The method of claim 1, wherein said selecting a performance level comprises:

selecting a highest performance level compatible with a constraint on maintaining a minimum idle thread utilization for a range of operation, a constraint on a minimum IC processor utilization, and a constraint on maximum IC processor utilization.

7. The method of claim 1, further comprising:

measuring IC processor utilization for each of said performance levels to determine a relationship between performance level and IC processor utilization.

8. The method of claim 1, wherein said software program comprises a software video encoder, said performance levels comprise encoding levels related to video quality, and said selecting comprises selecting an encoding level to achieve a highest possible video quality while maintaining IC processor utilization of said software video encoder within a desired range having a minimum IC processor utilization and a maximum IC processor utilization.

9. The method of claim 8, wherein said selecting said performance level further comprises:

maintaining a minimum idle thread utilization for a range of operating conditions.

10. The method of claim 9, wherein said minimum idle thread utilization is selected to facilitate another software program to start.

11. The method of claim 9, wherein said minimum idle thread utilization is selected to facilitate another software program to execute.

12. The method of claim 9, further comprising:

maintaining a minimum idle thread utilization for a range of operating conditions and maintaining IC processor utilization of said adjustable software program within a range of IC processor utilization having a minimum utilization and a maximum utilization.

13. The method of claim 1, further comprising:

in a startup mode of operation, selecting a minimum performance level as a starting performance level.

14. The method of claim 1, further comprising:

in a startup mode of operation, selecting a startup performance level of said adjustable software program to have a startup performance level with a processor utilization below a maximum IC processor utilization by a sufficient margin to accommodate differences in processor performance of at least two different types of IC processors.

15. A method of managing processor utilization in a video system, comprising:

providing a software video encoder having a plurality of encoding levels, each encoding level having a different associated processor utilization;

monitoring processor utilization of said software video encoder and of idle thread utilization; and

determining a greatest encoding level of said video encoder to maintain a minimum idle thread utilization for a range of operation conditions with processor utilization of said software video encoder within a desired range of processor utilization;

wherein said software video encoder automatically adjusts its encoding level to achieve the best video quality while maintaining idle thread utilization for other software programs over a range of operation.

16. The method of claim 15, wherein said minimum idle thread utilization is maintained until other of said software programs have a processor CPU utilization greater than a threshold utilization.

17. A computer system, comprising:

a software program resident on a memory, said software program having a plurality of performance levels associated with a quality of processing data on a processor, each performance level having a different associated processor utilization;

a processor usage monitor for monitoring processor utilization of said software program and idle thread utilization; and

a processor usage controller configured to select a highest performance level of said software program to provide highest quality data processing while maintaining processor usage of said software program within a desired range of utilization and maintaining a minimum idle thread utilization for a range of operating conditions.

18. The computer system of claim 17, wherein said software program is a video encoder.

19. The computer system of claim 18, wherein said system comprises a personal content recorder and said video encoder is adapted to record broadcast content.

20. A method of managing utilization of an integrated circuit (IC) processor, comprising:

monitoring processor utilization by an adjustable software program having at least two different performance levels associated with data processing throughput of said adjustable software program, wherein each performance level has a different associated IC processor utilization; and

selecting a performance level of said adjustable software program to maintain IC processor utilization for said adjustable software program within control constraints on IC processor utilization.